

Hit List

Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Clear

Generate Collection

Print

Fwd Refs

Bkwd Refs

Generate OACS

Search Results - Record(s) 1 through 5 of 5 returned.

☐ 1. Document ID: US 20040030745 A1

:- Invalid display element.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Des
------	-------	----------	-------	--------	----------------	------	-----------	-----------	-------------	--------	------	----------

☐ 2. Document ID: US 20030163801 A1

:- Invalid display element.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Des
------	-------	----------	-------	--------	----------------	------	-----------	-----------	-------------	--------	------	----------

☐ 3. Document ID: US 20030145310 A1

:- Invalid display element.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Des
------	-------	----------	-------	--------	----------------	------	-----------	-----------	-------------	--------	------	----------

☐ 4. Document ID: US 20030145282 A1

:- Invalid display element.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Des
------	-------	----------	-------	--------	----------------	------	-----------	-----------	-------------	--------	------	----------

☐ 5. Document ID: US 20030145281 A1

-: Invalid display element.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RWD	Draw Des
------	-------	----------	-------	--------	----------------	------	-----------	-----------	-------------	--------	-----	----------

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
-------	---------------------	-------	----------	-----------	---------------

Terms	Documents
((micro\$ or macro\$) with context\$) and (search\$ with ind\$) and database and (link\$ same (index or indices))	5

Display Format: [Change Format](#)

[Previous Page](#)

[Next Page](#)

[Go to Doc#](#)

First Hit Fwd Refs
End of Result Set

☐ **Generate Collection** **Print**

L37: Entry 2 of 2

File: USPT

Oct 30, 2001

US-PAT-NO: 6311214

DOCUMENT-IDENTIFIER: US 6311214 B1

TITLE: Linking of computers based on optical sensing of digital data

DATE-ISSUED: October 30, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rhoads; Geoffrey B.	West Linn	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Digimarc Corporation	Tualatin	OR			02

APPL-NO: 09/ 342689 [PALM]

DATE FILED: June 29, 1999

PARENT-CASE:

RELATED APPLICATION DATA This application is a continuation-in-part of copending application Ser. No. 09/130,624, filed Aug. 6, 1998, which is a continuation of application Ser. No. 08/508,083 filed on Jul. 27, 1995, (now U.S. Pat. No. 5,841,978). This application is also a continuation-in part of copending application Ser. No. 09/314,648, filed May 19, 1999 (attached as Appendix A). This application is also a continuation-in-part of copending provisional application 60/134,782, also filed May 19, 1999 (attached as Appendix B). This application is also a continuation-in-part of copending application Ser. No. 09/292,569, filed Apr. 15, 1999, which claims priority to application Ser. No. 60/082,228, filed Apr. 16, 1998.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 709/217; 709/313, 380/4

US-CL-CURRENT: 709/217; 380/255, 719/313

FIELD-OF-SEARCH: 709/217, 709/219, 709/227, 709/230, 709/250, 709/313, 709/328, 709/329, 380/4, 380/9, 380/49

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected

Search ALL

Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4947028</u>	August 1990	Gorog	
<input type="checkbox"/>	<u>5053956</u>	October 1991	Donald et al.	
<input type="checkbox"/>	<u>5262860</u>	November 1993	Fitzpatrick et al.	
<input type="checkbox"/>	<u>5288976</u>	February 1994	Citron et al.	
<input type="checkbox"/>	<u>5385371</u>	January 1995	Izawa	
<input type="checkbox"/>	<u>5463209</u>	October 1995	Figh et al.	
<input type="checkbox"/>	<u>5495581</u>	February 1996	Tsai	
<input type="checkbox"/>	<u>5496071</u>	March 1996	Walsh	
<input type="checkbox"/>	<u>5530852</u>	June 1996	Meske, Jr. et al.	
<input type="checkbox"/>	<u>5613004</u>	March 1997	Cooperman et al.	
<input type="checkbox"/>	<u>5640193</u>	June 1997	Wellner	
<input type="checkbox"/>	<u>5659164</u>	August 1997	Schmid et al.	
<input type="checkbox"/>	<u>5673316</u>	September 1997	Auerbach et al.	
<input type="checkbox"/>	<u>5721788</u>	February 1998	Powell et al.	
<input type="checkbox"/>	<u>5742845</u>	April 1998	Wagner	
<input type="checkbox"/>	<u>5761606</u>	June 1998	Wolzien	
<input type="checkbox"/>	<u>5761686</u>	June 1998	Bloomberg	
<input type="checkbox"/>	<u>5774664</u>	June 1998	Hidary et al.	
<input type="checkbox"/>	<u>5774666</u>	June 1998	Portuesi	
<input type="checkbox"/>	<u>5778102</u>	July 1998	Sandford, II et al.	
<input type="checkbox"/>	<u>5804803</u>	September 1998	Cragun et al.	
<input type="checkbox"/>	<u>5809317</u>	September 1998	Kogan et al.	
<input type="checkbox"/>	<u>5818441</u>	October 1998	Throckmorton et al.	
<input type="checkbox"/>	<u>5822432</u>	October 1998	Moskowitz et al.	
<input type="checkbox"/>	<u>5838458</u>	November 1998	Tsai	
<input type="checkbox"/>	<u>5848413</u>	December 1998	Wolff	707/10
<input type="checkbox"/>	<u>5857038</u>	January 1999	Owada et al.	
<input type="checkbox"/>	<u>5872589</u>	February 1999	Morales	
<input type="checkbox"/>	<u>5892900</u>	April 1999	Ginter et al.	
<input type="checkbox"/>	<u>5900608</u>	May 1999	Iida	
<input type="checkbox"/>	<u>5903729</u>	May 1999	Reber et al.	
<input type="checkbox"/>	<u>5905248</u>	May 1999	Russell et al.	235/462.27
<input type="checkbox"/>	<u>5913210</u>	June 1999	Call	
<input type="checkbox"/>	<u>5915027</u>	June 1999	Cox et al.	
<input type="checkbox"/>	<u>5918214</u>	June 1999	Perkowski	
<input type="checkbox"/>	<u>5932863</u>	August 1999	Rathus et al.	
<input type="checkbox"/>	<u>5933829</u>	August 1999	Durst et al.	

<input type="checkbox"/> <u>5938726</u>	August 1999	Reber et al.
<input type="checkbox"/> <u>5940595</u>	August 1999	Reber et al.
<input type="checkbox"/> <u>5978773</u>	November 1999	Hudetz et al.
<input type="checkbox"/> <u>5986651</u>	November 1999	Reber et al.
<input type="checkbox"/> <u>6012102</u>	January 2000	Shachar
<input type="checkbox"/> <u>6052486</u>	April 2000	Knowlton et al.
<input type="checkbox"/> <u>6081827</u>	June 2000	Reber et al.
<input type="checkbox"/> <u>6098106</u>	August 2000	Philyaw et al.
<input type="checkbox"/> <u>6108656</u>	August 2000	Durst et al.
<input type="checkbox"/> <u>6148331</u>	November 2000	Parry

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0493091	July 1992	EP	
WO95/14289	May 1995	WO	
WO95/20291	July 1995	WO	
WO96/27259	September 1996	WO	
WO96/36163	November 1996	WO	
WO97/02522	January 1997	WO	
WO97/43736	November 1997	WO	
WO98/03923	January 1998	WO	
WO98/51036	November 1998	WO	
WO99/57623	November 1999	WO	

OTHER PUBLICATIONS

U.S. application No. 60/000,442, Hudetz, filed Jun. 22, 1995.

IBM Technical Disclosure Bulletin 96A 61092, published Jan. 1, 1996.

"Distributing Uniform Resource Locators as Bar Code Images," IBM Technical Disclosure Bulletin, No. 39, No. 1, pp. 167-168, 96A 60059, published Jan. 1, 1996.

Frequently Asked Questions about Digimarc Signature Technology, Aug. 1, 1995, 9 pages.

Bartlett, et al., "An Overview of HighWater FBI Technology," Posted on Internet Mar. 22, 1996, 12 pages.

Digimarc presentation at RSA Conference, Jan. 1996, 4 pages.

"Digital Watermarks What Are They?" Digimarc Corporation, 1997.

Seybold Report on Internet Publishing, vol. 1, No. 4, Dec. 1996.

Seybold Report on Publishing Systems, vol. 25, No. 6, 1996.

Bethoney, "A Lasting Way For Artists To Leave Their Mark," PCWeek, Dec. 11, 1996.

Digital Media Monthly, Aug., 1996 (excerpt re Highwater FBI).

Digimarc Press Releases (various), 1996-1998.

Simone, "A Digital Watermark for Images," PC Magazine Dec. 18, 1996.

"Copyright Protection for Digital Images, Digital Fingerprinting from FBI," Highwater FBI brochure, 1995, 4 pages.

"Highwater FBI Limited Presentation, Image Copyright Protection Software," FBI Ltd brochure, Jul. 1995, 17 pages.

ART-UNIT: 214

PRIMARY-EXAMINER: Vu; Viet D.

ATTY-AGENT-FIRM: Conwell; William Y. Digimarc Corporation

ABSTRACT:

A printed object, such as an item of postal mail, a book, printed advertising, a business card, product packaging, etc., is steganographically encoded with plural-bit data. When such an object is presented to an optical sensor, the plural-bit data is decoded and used to establish a link to an internet address corresponding to that object.

23 Claims, 2 Drawing figures

First Hit Fwd Refs



Generate Collection

Print

L37: Entry 1 of 2

File: USPT

Nov 18, 2003

US-PAT-NO: 6650761

DOCUMENT-IDENTIFIER: US 6650761 B1

TITLE: Watermarked business cards and methods

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rodriguez; Tony F.	Portland	OR		
Rhoads; Geoffrey B.	West Linn	OR		
Davis; Bruce L.	Lake Oswego	OR		
Carr; J. Scott	Beaverton	OR		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Digimarc Corporation	Tualatin	OR			02

APPL-NO: 09/ 342688 [PALM]

DATE FILED: June 29, 1999

PARENT-CASE:

RELATED APPLICATION DATA This application is a continuation-in part of copending application Ser. No. 09/314,648, filed May 19, 1999 (attached as Appendix A). This application is also a continuation-in-part of copending provisional application Ser. No. 60/134,782, also filed May 19, 1999 (attached as Appendix B). The subject matter of this application is also related to that of the assignee's other patents and applications, as exemplified by U.S. Pat. No. 5,841,978.

INT-CL: [07] G06 K 9/00

US-CL-ISSUED: 382/100; 709/217

US-CL-CURRENT: 382/100; 709/217

FIELD-OF-SEARCH: 382/100, 709/217, 709/219, 380/234, 713/176

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected

Search ALL

Clear

PAT-NO

ISSUE-DATE

PATENTEE-NAME

US-CL



5337361

August 1994

Wang et al.

<input type="checkbox"/> <u>5493105</u>	February 1996	Desai	235/375
<input type="checkbox"/> <u>5559868</u>	September 1996	Blonder	379/96
<input type="checkbox"/> <u>5673316</u>	September 1997	Auerbach et al.	705/51
<input type="checkbox"/> <u>5742845</u>	April 1998	Wagner	710/11
<input type="checkbox"/> <u>5761686</u>	June 1998	Bloomberg	707/529
<input type="checkbox"/> <u>5765152</u>	June 1998	Erickson	
<input type="checkbox"/> <u>5778102</u>	July 1998	Sandford, II et al.	382/251
<input type="checkbox"/> <u>5804803</u>	September 1998	Cragun et al.	
<input type="checkbox"/> <u>5892900</u>	April 1999	Ginter et al.	713/200
<input type="checkbox"/> <u>5900608</u>	May 1999	Iida	235/381
<input type="checkbox"/> <u>5915027</u>	June 1999	Cox et al.	380/54
<input type="checkbox"/> <u>5932863</u>	August 1999	Rathus et al.	
<input type="checkbox"/> <u>5933829</u>	August 1999	Durst et al.	
<input type="checkbox"/> <u>5940595</u>	August 1999	Reber et al.	
<input type="checkbox"/> <u>5969324</u>	October 1999	Reber et al.	235/462.13
<input type="checkbox"/> <u>5978773</u>	November 1999	Hudetz et al.	
<input type="checkbox"/> <u>6012102</u>	January 2000	Shachar	
<input type="checkbox"/> <u>6052486</u>	April 2000	Knowlton et al.	382/232
<input type="checkbox"/> <u>6138151</u>	October 2000	Reber et al.	709/219
<input type="checkbox"/> <u>6297491</u>	October 2001	Mangerson	250/208.1
<input type="checkbox"/> <u>6311214</u>	October 2001	Rhoads	709/217
<input type="checkbox"/> <u>6314457</u>	November 2001	Schena et al.	
<input type="checkbox"/> <u>6332193</u>	December 2001	Glass et al.	713/170
<input type="checkbox"/> <u>6345104</u>	February 2002	Rhoads	
<input type="checkbox"/> <u>2001/0001854</u>	May 2001	Schena et al.	

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0493091	July 1992	EP	
WO 97/43736	November 1997	WO	

OTHER PUBLICATIONS

U.S. patent application Ser. No. 60/112,955, Rhoads, filed Dec. 18, 1998.
U.S. patent application Ser. No. 09/074,034, Rhoads, filed May 6, 1998.
U.S. patent application Ser. No. 09/185,380, Davis et al., filed Nov. 3, 1998.
U.S. patent application Ser. No. 09/302,663, Gustafson et al., filed Apr. 30, 1999.

U.S. patent application Ser. No. 09/314,648, Rodriguez et al., filed May 19, 1999.
U.S. patent application Ser. No. 09/465,418, Rhoads et al., filed Dec. 16, 1999.

ART-UNIT: 2625

PRIMARY-EXAMINER: Patel; Jayanti K.

ASSISTANT-EXAMINER: Choobin; M. Barry

ATTY-AGENT-FIRM: Conwell; William Y. Digimarc Corporation

ABSTRACT:

A person's business card is steganographically encoded with plural-bit data. When presented to a computer system with an optical sensor, the plural-bit data is decoded and used to trigger various functionality. For example, the system can link to a remote data store containing updated contact information for the person--contact information that is updated during the day as the person's activities make different contact information appropriate at different times. A great variety of other arrangements, some employing other steganographically encoded objects, are also detailed.

5 Claims, 2 Drawing figures

L30: Entry 2 of 2

File: USPT

Apr 28, 1998

DOCUMENT-IDENTIFIER: US 5745727 A

TITLE: Linked caches memory for storing units of information

Abstract Text (1):

A method and apparatus for linking two independent caches which have related information stored therein. Each unit of information stored in a first cache memory is associated with one unit of information stored in the second cache memory. Each unit of information stored in the first cache memory includes a pointer or index to the associated information unit in the second cache memory. Each information unit stored in the second cache is only stored once, regardless of the number of units in the first cache that are associated with a particular unit within the second cache. Therefore, even if more than one unit of information within the first cache memory is associated with the same unit of information within the second cache memory, that unit of information stored in the second cache memory is only stored once.

Application Filing Date (1):

19970415

Brief Summary Text (11):

The present invention is a method and apparatus for linking two independent caches which have related information stored therein. In the present invention, each unit of information stored in a first cache memory is associated with one unit of information stored in the second cache memory. Each unit of information stored in the first cache memory includes an index to the associated information unit in the second cache memory. Accordingly, the caches are "linked". By using two linked caches, the total amount of cache memory is reduced in systems in which there would be redundancy in the information that is stored in second cache. In such systems, redundancy is the result of some of the information units stored in the second cache being associated with more than one information unit stored in the first cache.

Brief Summary Text (13):

If a requesting device requests a block of information, a first cache controller searches the first cache to determine whether the Exchange Context is present in the first cache. If the Exchange Context is not present in the first cache, then the first cache controller informs a coordination control logic device to request that a microcontroller read the Exchange Context from a main context memory array (i.e., a "context array"). The Exchange Context information read from the context array is stored in the first cache. In accordance with the present invention, the Port Context Index in the first cache is used to direct the second cache controller to associated Port Context information within the second cache. That is, the Port Context Index is communicated from the first cache to the second cache controller. The second cache controller then attempts to locate the Port Context information associated with the Exchange Context retrieved from the first cache. If the Port Context information is found, then both the Port Context information and the Exchange Context information are presented to the requesting device.

Detailed Description Text (14):

If there is a miss in the first cache 103, then the first cache controller 105 signals the coordination controller 110 that a miss has occurred via signal line 129. In response, the coordination controller 110 determines whether there is a location available in the first cache 103 to store the requested Exchange Context. If not, then the coordination controller saves an Exchange Context from the cache into the context array 112, preferably using a direct memory access (DMA) operation into the context array 112 within the memory 107 via signal lines 131. Once space has been cleared within the first cache 103, the coordination controller 110 preferably performs a DMA read operation from the context array 112 within the memory 107 via signal lines 131 to read the Exchange Context associated with the frame received by the protocol management engine 113. If that frame is the first frame to be received by the communications adapter 100, then the coordination controller 110 will not find the Exchange Context in the context array 112. Therefore, the coordination controller 110 interrupts the microcontroller 101 via signal line 133. The microcontroller 101 negotiates an Exchange Context to be associated with each frame of that Exchange that is received in the future. In the process of negotiating the Exchange Context, the microcontroller 101 indicates which device will be the originator for the Exchange.

Detailed Description Text (15):

In accordance with the preferred embodiment of the present invention, the microcontroller 101 assigns a PCI as a part of the Exchange Context. If the port from which the frame originated had previously communicated with the communications adapter 100, then a Port Context will already have been negotiated. Accordingly, the same Port Context will be used that was previously used between that port and the communications adapter 100.

Detailed Description Text (17):

Once the microcontroller 101 has completed the Exchange Context for that Exchange, the microcontroller 101 stores the Exchange Context in the context array 112 and sends the coordination controller 110 a copy of the Exchange Context to be stored in the first cache 103. Alternatively, the microcontroller 101 signals the coordination controller 110 to read the Exchange Context directly from the context array 112 in a DMA operation. The coordination controller 110 then applies the Exchange Context to a Write Path Controller 115. The Write Path Controller 115 is a state machine which controls the input to each of the two caches 103, 109. The Write Path Controller 115 prioritizes write operations to each cache 103, 109. That is, three different components may write to each cache 103, 109. The coordination controller 110 has the highest priority to write to each cache 103, 109. The protocol management engine 113 has the next highest priority to write to each cache 103, 109. The microcontroller 101 has the lowest priority to write to each cache 103, 109. The Write Path Controller 115 determines whether a device of higher priority is attempting to write to the cache concurrently. If so, then that device is allowed to write to each cache 103, 109 first. Since the coordination controller 110 has the highest priority, the coordination controller 110 writes the Exchange Context to the first cache 103 without delay, unless one of the other devices is already writing data to the first cache 103. The Write Path Controller 115 activates the write strobe to the cache 103, 109 to which the coordination controller 110 is writing via signal line 132 or 134 depending upon which cache 103, 109 is being written. The activation of the strobe to the cache is also coupled to the coordination controller 110 via signal line 135 as an acknowledgement that the write operation has been completed.

Detailed Description Text (19):

If the Port Context is not found within the second cache 109, then the second cache controller 111 signals the coordination controller 110. The coordination controller 110 then ensures that a location in the second cache 109 is present within the second cache 109 for the requested Port Context by performing a DMA write of one of the Port Context already in the second cache 109 into the context array 112, if no

location is available. The coordination controller 110 then attempts to find the Port Context within the context array 112. If the PCI is not currently associated with a Port Context (i.e., the PCI was created for this frame when the Exchange Context was generated), then the coordination controller 110 interrupts the microprocessor 101. The microcontroller 101 negotiates a Port Context and stores that Port Context in a location within the context array 112 that is associated with that PCI. The microcontroller 101 then sends a copy of the Port Context to the coordination controller 110 to be stored within the second cache 109. Alternatively, the microcontroller 101 signals the coordination controller 110 to perform a DMA read operation into the context array 112 to attempt again to read the Port Context.

Detailed Description Text (22):

If the Port Context associated with the PCI is not present in the second cache 109, then the coordination controller 110 performs a DMA read to the context array 112. If the Port Context is not present in the context array 112, then the microcontroller 101 generates a new Port Context. In either case, the Port Context is provided to the coordination controller 110 and stored in the second cache 109. The second cache controller 111 again attempts to find the Port Context and signals a hit to the coordination controller 110. The coordination controller 110 then causes both the Exchange Context and the Port Context to be provided to the protocol management engine 113.

Detailed Description Text (24):

Returning to STEP 303, if the Exchange Context is not found, then the cache controller signals the coordination controller 110 to read the Exchange Context from the context array 112 (STEP 311). If the Exchange Context is not present within the context array 112, then the microcontroller 101 is interrupted and negotiates an Exchange Context (STEP 313). The Exchange Context is stored in the context array 112 (STEP 315). The process then returns to STEP 311 and the coordination controller 110 again attempts to read the Exchange Context from the context array 112 (STEP 311). This time the Exchange Context will be present. When the Exchange Context is found within the context array 112, the Exchange Context is stored in the first cache 103 (STEP 315). The first cache controller 105 then once again attempts to find the Exchange Context within the first cache 103 (STEP 303). This time the Exchange Context will be found. When the Exchange Context is found within the first cache 103, the process continues as described above.

Detailed Description Text (25):

If in STEP 307 the Port Context is not present in the second cache 109, then the coordination controller 110 is signalled and attempts to find the Port Context within the context array 112 (STEP 317). If the Port Context is present in the context array 112, then the Port Context is stored in the second cache 109 (STEP 319). If the Port Context is not present in the context array 112, then the coordination controller 110 interrupts the microcontroller 101 to negotiate a new Port Context (STEP 321). The Port Context is then stored in the second cache 109 (STEP 319). Once the Port Context is stored within the second cache 109, the second cache controller 111 again attempts to find the Port Context (STEP 307). The process then continues as described above.

Detailed Description Text (28):

If the microcontroller 101 attempts to read the from either cache 103, 109, the information must be searched by the appropriate cache controller 105, 111. The coordination controller 110 transfers the information to the microcontroller 101. For example, the microcontroller 101 may request an Exchange Context from the first cache 103 through the first cache controller 105. The information is provided to the coordination controller 110, which saves the information into the microcontroller 101 memory 107, or alternatively, into a register in the microcontroller 101.

Detailed Description Text (30):

A number of embodiments of the present invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, the linked caches of the present invention may be used in any system in which a cache is used to store first units of information associated with a second unit of information. For example, in a database in which addresses are stored in a cache, the street address may be stored in a first cache with an index into a second cache which stores the city, state, and zip code associated with the address. Accordingly, any device may be coupled to the linked caches and the coordination controller 110 to request that information be read from the linked caches.

CLAIMS:

1. A linked cache memory for storing units of information, the units of information being a first and second subset of units of information stored in a related memory device, including:

- (a) a first cache device for storing the first subset of the information;
- (b) a second cache device for storing the second subset of the information;
- (c) a cache controller, coupled to the first and second cache devices for:
 - (1) receiving from an external device a first index;
 - (2) searching the first cache device for a first unit of information associated with the first index;
 - (3) outputting a first indication that the first unit of information was found, if the first unit of information is presently stored within the first cache device;
 - (4) receiving from the first cache device a second index embedded within the first unit of information;
 - (5) searching the second cache device for a second unit of information associated with the second index; and
 - (6) outputting a second indication that the second unit of information was found, if the second unit of information is present within the second cache device;
- (d) a coordination controller, coupled to the cache controller, for receiving from the cache controller the first and second indications that the first and second cache devices have found the first and second units of information, and in response to such receipt of such indications, enabling outputting of the first and second units of information; and
- (e) a write path controller, coupled to the coordination controller and the first and second cache devices, for coupling input signals from one of a plurality of sources to inputs of the first or the second cache, and for indicating to the source of the input signal that input data represented by the input signal has been stored in a cache device.

4. A linked cache memory for storing units of information, the units of information being a first and second subset of units of information stored in a related memory device, including:

- (a) a first cache device for storing the first subset of the information;
- (b) a second cache device for storing the second subset of the information;

(c) a cache controller, coupled to the first and second cache devices for:

(1) receiving from an external device a first index;

(2) searching the first cache device for a first unit of information associated with the first index;

(3) outputting a first indication that the first unit of information was found, if the first unit of information is presently stored within the first cache device;

(4) receiving from the first cache device a second index embedded within the first unit of information;

(5) searching the second cache device for a second unit of information associated with the second index; and

(6) outputting a second indication that the second unit of information was found, if the second unit of information is present within the second cache device;

(d) a coordination controller, coupled to the cache controller, for receiving from the cache controller the first and second indications that the first and second cache devices have found the first and second units of information, and in response to such receipt of such indications, enabling outputting of the first and second units of information, wherein the coordination controller is capable of performing a direct memory access operation to read information from the related memory device.

5. A linked cache memory for storing units of information, the units of information being a first and second subset of units of information stored in a related memory device, including:

(a) a first cache device for storing the first subset of the information;

(b) a second cache device for storing the second subset of the information;

(c) a cache controller, coupled to the first and second cache devices for:

(1) receiving from an external device a first index;

(2) searching the first cache device for a first unit of information associated with the first index;

(3) outputting a first indication that the first unit of information was found, if the first unit of information is presently stored within the first cache device;

(4) receiving from the first cache device a second index embedded within the first unit of information;

(5) searching the second cache device for a second unit of information associated with the second index; and

(6) outputting a second indication that the second unit of information was found, if the second unit of information is present within the second cache device;

(d) a coordination controller, coupled to the cache controller, for receiving from the cache controller the first and second indications that the first and second cache devices have found the first and second units of information, and in response to such receipt of such indications, enabling outputting of the first and second units of information; and

(e) a lock means for locking the first and second cache devices to prevent a particular unit of information from being altered when that unit of information is in use;

wherein the first unit of information is an exchange context and the second unit of information is a port context, the exchange context and the port context being associated with a frame of data which is either being transmitted or received, and wherein the lock means activates a receive lock bit when a port context or exchange context is being used in association with a received frame.

6. A linked cache memory for storing units of information, the units of information being a first and second subset of units of information stored in a related memory device, including:

- (a) a first cache device for storing the first subset of the information;
- (b) a second cache device for storing the second subset of the information;
- (c) a cache controller, coupled to the first and second cache devices for:
 - (1) receiving from an external device a first index;
 - (2) searching the first cache device for a first unit of information associated with the first index;
 - (3) outputting a first indication that the first unit of information was found, if the first unit of information is presently stored within the first cache device;
 - (4) receiving from the first cache device a second index embedded within the first unit of information;
 - (5) searching the second cache device for a second unit of information associated with the second index; and
 - (6) outputting a second indication that the second unit of information was found, if the second unit of information is present within the second cache device;
- (d) a coordination controller, coupled to the cache controller, for receiving from the cache controller the first and second indications that the first and second cache devices have found the first and second units of information, and in response to such receipt of such indications, enabling outputting of the first and second units of information; and
- (e) a lock means for locking the first and second cache devices to prevent a particular unit of information from being altered when that unit of information is in use;

wherein the first unit of information is an exchange context and the second unit of information is a port context, the exchange context and the port context being associated with a frame of data which is either being transmitted or received, and wherein the lock means activates a transmit lock bit when a port context or exchange context is being used in association with a frame to be transmitted.

7. A communications adapter within a host, for receiving and transmitting frames of data, including:

- (a) a memory device for storing context data including exchange context information and port context information;

- (b) a first cache device having shorter read times than the memory device, for storing a subset of the exchange context information;
- (c) a second cache device having shorter read times than the memory device, for storing a subset of the port context information;
- (d) a cache controller, coupled to the first and second cache device for:
 - (1) receiving from an external device a first index;
 - (2) searching the first cache device for an exchange context associated with the first index;
 - (3) outputting a first indication that the exchange context was found, if the exchange context being associated with the first index is presently stored within the first cache device;
 - (4) receiving from the first cache device a second index embedded within the exchange context;
 - (5) searching the second cache device for a port context associated with the second index; and
 - (6) outputting a second indication that the port context associated with the second index was found, if the port context is present within the second cache device;
- (e) a coordination controller, coupled to the cache controller, for receiving from the cache controller the first and second indications that the first and second cache devices have found the exchange context and port context associated with the first and second index, and enabling outputting of the exchange context and port context in response to receiving both the first and second indications; and
- (f) a microcontroller, coupled to the memory device and to the coordination controller, for generating exchange context and port context information to be stored within the memory device upon receipt of a request from the coordination controller, and for directly writing to the first and second cache device.

11. A method for storing and retrieving units of information in a linked cache device having a first memory device and a second memory device, and a cache controller, the first and second memory devices each having units of information stored within that are a first and second subset, respectively, of units of information stored in a related external memory device, including the steps of:

- (a) receiving from an external control device a first index;
- (b) searching the first memory device for a first unit of information associated with the first index;
- (c) communicating a first indication that the first unit of information was found, if the first unit of information is presently stored within the first cache device;
- (d) receiving from the first memory device a second index embedded within the first unit of information;
- (e) searching the second cache device for a second unit of information associated with the second index;
- (f) outputting a second indication that the second unit of information was found, if the second unit of information is present within the second cache device;

(g) if the first unit of information associated with the first index is not present in the first cache device, then:

(1) performing a direct memory access operation into the related external memory device to read the first unit of information associated with the first index and store that first unit of information in the first cache device;

(2) communicating a first indication that the first unit of information associated with the first cache device is presently within the first cache device;

(h) if the second unit of information associated with the second index is not present in the second cache device, then:

(1) performing a direct memory access operation into the related external memory device to read the second unit of information associated with the second index and store that second unit of information in the second cache device; and

(2) communicating a second indication that the second unit of information associated with the second cache device is presently within the second cache device.

12. A method for storing and retrieving units of information in a linked cache device having a first memory device and a second memory device, and a cache controller, the first and second memory devices each having units of information stored within that are a first and second subset, respectively, of units of information stored in a related external memory device, including the steps of:

(a) receiving from an external control device a first index;

(b) searching the first memory device for a first unit of information associated with the first index;

(c) communicating a first indication that the first unit of information was found, if the first unit of information is presently stored within the first cache device;

(d) receiving from the first memory device a second index embedded within the first unit of information;

(e) searching the second cache device for a second unit of information associated with the second index;

(f) outputting a second indication that the second unit of information was found, if the second unit of information is present within the second cache device;

(g) receiving from the cache controller the first and second indications that the first and second cache devices have found the first and second unit of information;

(h) enabling outputting of the first and second unit of information in response to receiving both the first and second indications; and

(i) performing a direct memory access operation to read information from the external memory device.

13. A method for storing and retrieving units of information in a linked cache device having a first memory device and a second memory device, and a cache controller, the first and second memory devices each having units of information stored within that are a first and second subset, respectively, of units of

information stored in a related external memory device, including the steps of:

- (a) receiving from an external control device a first index;
- (b) searching the first memory device for a first unit of information associated with the first index, the first unit of information being an exchange context;
- (c) communicating a first indication that the first unit of information was found, if the first unit of information is presently stored within the first cache device;
- (d) receiving from the first memory device a second index embedded within the first unit of information;
- (e) searching the second cache device for a second unit of information associated with the second index, the second unit of information being a port context;
- (f) outputting a second indication that the second unit of information was found, if the second unit of information is present within the second cache device;
- (g) receiving from the cache controller the first and second indications that the first and second cache devices have found the first and second unit of information;
- (h) enabling outputting of the first and second unit of information in response to receiving both the first and second indications; and
- (i) locking the first and second memory devices to prevent a particular unit of information from being altered when that unit of information is in use;
- (j) associating the exchange context and the port context with a frame of data which is either being transmitted or received; and
- (k) activating a receive lock bit when the port context or the exchange context is being used in association with a received frame.

14. A method for storing and retrieving units of information in a linked cache device having a first memory device and a second memory device, and a cache controller, the first and second memory devices each having units of information stored within that are a first and second subset, respectively, of units of information stored in a related external memory device, including the steps of:

- (a) receiving from an external control device a first index;
- (b) searching the first memory device for a first unit of information associated with the first index, the first unit of information being an exchange context;
- (c) communicating a first indication that the first unit of information was found, if the first unit of information is presently stored within the first cache device;
- (d) receiving from the first memory device a second index embedded within the first unit of information;
- (e) searching the second cache device for a second unit of information associated with the second index, the second unit of information being a port context;
- (f) outputting a second indication that the second unit of information was found, if the second unit of information is present within the second cache device;

(g) receiving from the cache controller the first and second indications that the first and second cache devices have found the first and second unit of information;

(h) enabling outputting of the first and second unit of information in response to receiving both the first and second indications; and

(i) locking the first and second memory devices to prevent a particular unit of information from being altered when that unit of information is in use;

(j) associating the exchange context and the port context with a frame of data which is either being transmitted or received; and

(k) activating a transmit lock bit when the port context or the exchange context is being used in association with a frame to be transmitted.

WEST Search History

Hide Items

Restore

Clear

Cancel

DATE: Friday, February 20, 2004

Hide?	Set Name	Query	Hit Count
		<i>DB=PGPB,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES; OP=OR</i>	
<input type="checkbox"/>	L41	((micro\$ or macro\$) with context\$) and (search\$ with ind\$) and database and (link\$ same (index or indices))	5
<input type="checkbox"/>	L40	=19990803 and (link\$ same (index or indices))	0
<input type="checkbox"/>	L39	=19990803 and (link\$ with (index or indices))	0
<input type="checkbox"/>	L38	=19990803 and (link\$ with (index or indices)) and database	0
		<i>DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=OR</i>	
<input type="checkbox"/>	L37	I36 and (search\$ with Internet)	2
<input type="checkbox"/>	L36	L33 and (link\$ with (index or indices)) and database	2
<input type="checkbox"/>	L35	L34 and (updat\$ with (data or information))	3
<input type="checkbox"/>	L34	L33 and (index or indices) and database	5
<input type="checkbox"/>	L33	I32 and (search\$ with Internet)	16
<input type="checkbox"/>	L32	=19990803	28
<input type="checkbox"/>	L31	L29 and (track\$ with (navigati\$ or surf\$ or search\$) with Internet)	0
<input type="checkbox"/>	L30	L29 and (link\$ with ind\$)	2
<input type="checkbox"/>	L29	=19990803	36
<input type="checkbox"/>	L28	L27 and ((match\$ or search\$) with ind\$)	0
<input type="checkbox"/>	L27	L25 or I22	2
<input type="checkbox"/>	L26	L25 or I2	1091
<input type="checkbox"/>	L25	(micro adj context\$) and (macro adj context\$)	1
<input type="checkbox"/>	L24	micro-context and macro-context	0
<input type="checkbox"/>	L23	microcontext and macrocontext	0
<input type="checkbox"/>	L22	6453356.pn.	1
<input type="checkbox"/>	L21	L20 and ((control\$ or select\$) with speed\$)	9
<input type="checkbox"/>	L20	L19 and (auction\$ or bid\$)	9
<input type="checkbox"/>	L19	L18 and ((image or picture) with speed)	92
<input type="checkbox"/>	L18	=20011112	106
		<i>DB=PGPB,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES; OP=OR</i>	
<input type="checkbox"/>	L17	I15 not L16	10
<input type="checkbox"/>	L16	L15 and (auction\$ or bid\$)	1
<input type="checkbox"/>	L15	L14 and link\$	11



Merriam-Webster
OnLine

Merriam-Webster FOR KIDS

Encyclopedia BRITANNICA

Merriam-Webster ONLINE

Merriam-Webster COLLEGIATE

Merriam-Webster UNABRIDGED

Merriam-Webster Online Dictionary

Thesaurus

12 entries found for **corpus**. The first 10 are listed below.

To select an entry, click on it. For more results, [click here](#).

corpus

corpus allatum

corpus callosum

corpus cardiacum

Corpus Christi

corpus delicti

Go

corpus
corpus allatum corpus callosum corpus cardiacum
Corpus Christi corpus delicti corpus luteum corpus
striatum habeas corpus habeas corpus ad
subjiendum

Main Entry: **cor·pus**

Pronunciation: 'kor-p&s

Function: *noun*

Inflected Form(s): *plural cor·po·ra*

/-p (&-) r&/

Etymology: Middle English, from Latin

1 : the body of a human or animal especially when dead

2 a : the main part or body of a bodily structure or organ corpus of the uterus > **b** : the main body or corporeal substance of a thing; *specifically* : the principal of a fund or estate as distinct from income or interest

3 a : all the writings or works of a particular kind or on a particular subject; *especially* : the complete works of an author **b** : a collection or body of knowledge or evidence; *especially* : a collection of recorded utterances used as a basis for the descriptive analysis of a language

Get the **Top 10 Search Results for "corpus"**

For **More Information on "c rpus"** go to Britannica.com

Pronunciation Symbols

Merriam-Webster Online

Dictionary

Thesaurus

Go



SEARCH

Find Find

Palm & Pocket PC

Browse and download Merriam-Webster e-books and games for Palm and Pocket PC PDAs and Mobile Phones

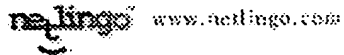
[Merriam-Webster Online Store](#)

Handheld Collegiate

Now you can take the Eleventh Edition with you anywhere as Franklin's new Speaking Electronic Handheld!

Franklin.com/estore

Merriam-Webster
Collegiate
14-day Free Trial



microcontent

Web page content that describes what's on the Web site or directs users to another section. For example, titles, subtitles, navigation links, paragraph blurbs, and copyright statements. The microcontent on a Web site's "Thank You" page (which appears after a user fills out a form) should always include the company's phone number, a link to the [FAQ](#) section, and information about when the user can expect to receive a reply.

NetLingo Classification: Online Business term



done!

E-mail this Term to a Friend!

show me some more words!

NetLingo Partner Links: [Online College Degree Programs](#) | [Online Schools](#) | [Online Coupons](#)
[Dell Coupons](#) | [Amazon Coupons](#) | [HP Laptop](#) | [Running Clothing](#) | [Brand Name Apparel](#)
[Sports Equipment](#) | [Discount Vitamins](#) | [Plus Size Clothing](#) | [Skin Care](#)
[Home Equity Loans](#) | [Search for Credit Cards](#) | [Play Poker](#)

[Home](#) | [The Dictionary](#) | [Buy the NetLingo Book here!](#) | [Smiley Gift Store](#) :^)

Copyright © 1995-2004 [Erin Jansen](#) All rights reserved.
Reproduction in whole or in part requires permission. [Privacy policy](#)

First Hit Fwd Refs

End of Result Set

☐ **Generate Collection** **Print**

L25: Entry 1 of 1

File: USPT

Nov 11, 2003

US-PAT-NO: 6647301

DOCUMENT-IDENTIFIER: US 6647301 B1

TITLE: Process control system with integrated safety control system

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sederlund; Edward R.	Saginaw	MI		
Quelle; Ernst W.	Stade			DE
Bezecny; Helmut A.	Duedenbuettel			DE
Kanse; Johannes C.	Biervliet			NL
Lindesmith; Robert J.	Midland	MI		
Clement; John L.	Midland	MI		
Grinwis; Donald	Midland	MI		
Baca, Jr.; Eloy	Attleboro	MA		
Dunlap; Dennis J.	Attleboro	MA		
Frank; Brent M.	Franklin	MA		
Tibazarwa; Augustine K.	Quincy	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Dow Global Technologies Inc.	Midland	MI			02

APPL-NO: 09/ 482386 [PALM]

DATE FILED: January 12, 2000

PARENT-CASE:

CROSS-REFERENCE TO PRIOR APPLICATION This application claims the benefit of U.S. Provisional Application No. 60/130,627 filed Apr. 22, 1999.

INT-CL: [07] G05 B 9/02

US-CL-ISSUED: 700/79; 700/20, 700/21, 700/174, 700/108, 700/110, 714/6, 714/7, 714/8, 714/15, 714/24, 714/31, 714/47

US-CL-CURRENT: 700/79; 700/108, 700/110, 700/174, 700/20, 700/21, 714/15, 714/24, 714/31, 714/47, 714/6, 714/7, 714/8

FIELD-OF-SEARCH: 700/20, 700/21, 700/174, 700/108, 700/110, 700/79, 714/47, 714/15, 714/24, 714/6, 714/7-8, 714/31

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected

Search ALL

Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>4598355</u>	July 1986	Shepler et al.	700/79
<input type="checkbox"/> <u>4649515</u>	March 1987	Thompson et al.	706/52
<input type="checkbox"/> <u>5151866</u>	September 1992	Glaser et al.	364/483
<input type="checkbox"/> <u>5408603</u>	April 1995	Van de Lavoir et al.	395/161
<input type="checkbox"/> <u>5428745</u>	June 1995	de Bruijn et al.	395/200
<input type="checkbox"/> <u>5428769</u>	June 1995	Glaser et al.	395/575
<input type="checkbox"/> <u>5491625</u>	February 1996	Pressnall et al.	364/133
<input type="checkbox"/> <u>5506792</u>	April 1996	Adelson et al.	364/570
<input type="checkbox"/> <u>5519603</u>	May 1996	Allbery, Jr. et al.	364/133
<input type="checkbox"/> <u>5553237</u>	September 1996	Eisenberg et al.	395/184.01
<input type="checkbox"/> <u>5555424</u>	September 1996	Sederlund et al.	395/800
<input type="checkbox"/> <u>5561770</u>	October 1996	de Bruijn et al.	395/200.06
<input type="checkbox"/> <u>5568615</u>	October 1996	Sederlund et al.	395/200.08
<input type="checkbox"/> <u>5572671</u>	November 1996	Eisenberg et al.	395/184.01
<input type="checkbox"/> <u>5583757</u>	December 1996	Baca, Jr. et al.	364/184
<input type="checkbox"/> <u>5631825</u>	May 1997	van Weele et al.	364/188
<input type="checkbox"/> <u>5655133</u>	August 1997	Dupree et al.	395/800.23
<input type="checkbox"/> <u>5726668</u>	March 1998	Clement	345/1
<input type="checkbox"/> <u>5864657</u>	January 1999	Stiffler	714/15
<input type="checkbox"/> <u>5984504</u>	November 1999	Doyle et al.	700/108

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0457308	November 1991	EP	
WO 93/13477	July 1993	WO	
WO 98/36355	August 1998	WO	

OTHER PUBLICATIONS

Distributed Computing Environment Using Real-Time Scheduling Logic and Time Deterministic Architecture, filed in the United States of America on May 26, 1998, Application Ser. No. 60/086,737, Woods et al.

Specification for Limits and methods of measurement of radio disturbance characteristics of industrial, scientific and medical (ISM) radio-frequency equipment, British Standard, BS EN 55011:1991.

Electromagnetic compatibility--Generic emission standard, Part 2. Industrial

environment, British Standard, BS EN 50081-2:1994.

British Standard Specification for Limits and methods of measurement of radio interference characteristics of information technology equipment, British Standard, BS 6527:1988 EN 55022:1987.

Limits and methods of measurements of radio disturbance characteristics of information technology equipment, British Standard, BS EN 55022:1995 CISPR 22:1993.

Safety requirements for electrical equipment for measurement, control, and laboratory use, Part 1. General requirements, British Standard, BS EN 61010-1:1993.

Automatic gas burner control systems for gas burner and gas burnings appliances with or without fans, British Standard, BS EN 298:1994.

Technical Help to Exporters (translation), Electrical equipment for furnaces, British Standards Institution, DIN VDE 0116, Oct. 1989.

Principles for computers in safety-related systems (translation), DIN V VDE 0801 Amendment A1, Revision: 0.7 Nov. 25, 1994.

Commission Electrotechnique Internationale, International Electrotechnical Commission, Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 1: General requirements, CEI IEC 61508-1, Version 4.0 May 12, 1997.

Commission Electrotechnique Internationale, International Electrotechnical Commission, Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 2: Requirements for electrical/electronic/programmable electronic safety-related systems, CEI IEC 61508-2, Version 4.0 May 12, 1997.

Commission Electrotechnique Internationale, International Electrotechnical Commission, Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 3: Software requirements, CEI IEC 61508-3, Version 12.0 May 12, 1997.

Commission Electrotechnique Internationale, International Electrotechnical Commission, Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 4: Definitions and abbreviations, CEI IEC 61508-4, Version 4.0 May 12, 1997.

Commission Electrotechnique Internationale, International Electrotechnical Commission, Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 5: Examples of methods for the determination of safety Integrity levels, CEI IEC 61508-5, Version 4.0 May 12, 1997.

Commission Electrotechnique Internationale, International Electrotechnical Commission, Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 6: Guidelines on the application of parts 2 and 3, CEI IEC 61508-6, Version 4.0 May 12, 1997.

Commission Electrotechnique Internationale, International Electrotechnical Commission, Functional safety of electrical/electronic/programmable electronic safety-related systems, Part 7: Overview of techniques and measures, CEI IEC 61508-7, Version 4.0 May 12, 1997.

Measurement-Control-Regulation, Fundamental Safety Considerations for MSR Protection Equipment, English title: Measurement and control: Fundamental safety aspects to be considered for measurement and control equipment, DIN V 19 250 (translation included).

Code of Federal Regulations, Labor, 29, Part 1900 to .sctn. 1910.999, Revised as of Jul. 1, 1998.

Code of Federal Regulations, Labor, 29, Part 1900 to .sctn. 1910.999, Revised as of Jul. 1, 1999.

Lexis Law Publishings Code of Federal Regulations, 29 CFR 1910.119, Feb. 8, 2000.

Leonard Sterle, Applying PLCs in Safety Systems, 74 Control and Instrumentation, 23 (1991)Jan., No. 1, pp. 39-40, London, GB.

Patent Abstracts of Japan, JP 09185556, Jul. 15, 1997, Toshiba Corp., Method for Managing Duplex Memory and Duplex Memory Management Device.

PRIMARY-EXAMINER: Gordon; Paul P.

ASSISTANT-EXAMINER: Pham; Thomas

ABSTRACT:

A process control system receiving input signals from a controlled apparatus and using the input signals in determining at least one output signal modifying the characteristics of at least one respective control device in the controlled apparatus where the source code for the general control of the apparatus and the source code for the safety shutdown system of the apparatus are compiled to control code in a unified compilation.

8 Claims, 95 Drawing figures

First Hit Fwd Refs

End of Result Set

☐ [Generate Collection](#) [Print](#)

L25: Entry 1 of 1

File: USPT

Nov 11, 2003

DOCUMENT-IDENTIFIER: US 6647301 B1

TITLE: Process control system with integrated safety control system

Detailed Description Text (31):

In introduction of the control-computer-executed logic and the use of the aforementioned SEQUENCE object in a control computer program in the preferred embodiment, a brief review of two terms related to the art and technology of chemical engineering is in order. Traditional concepts of the "unit operation" (a particular kind of physical change procedure used and effected in chemical processing--for example, filtration, evaporation, distillation, or heat transfer) and the "unit process" (a particular kind of transformation in materials via chemical reaction--for example, oxidation, hydrolysis, esterification, polymerization, or nitration) define functional activities which must execute in order to effect a particular desired incremental transformation of a "starting" material to a "product" material. These physical changes and chemical transformations usually occur through use of an apparatus which, in operation, converts starting material into product material (in both a micro and macro context), and it is useful for that portion of the apparatus involved in the execution of at least one "unit operation" or "unit process" to be referenced and organized for control purposes in the described embodiment in a least one "Process Unit" (for example, a reactor, a fractionating tower, a crystallizer, a dryer, a tank farm, a distillation unit, an extraction unit, or an evaporator). In an overall chemical manufacturing plant a number of sequential and parallel "unit operations" and "unit processes" are therefore effectively executed collectively in a respective set of "Process Units" to convert many instances of "starting materials" into "product materials" (where the "product material" from one "Process Unit" is very often the "starting material" for the next "Process Unit" when the situation is examined in a micro context). Engineering and operations personnel have traditionally referenced and managed the operation of such a plant apparatus in the context of a set of such "Process Units" in effecting operation of these sequential and parallel "unit operations" and "unit processes" where "raw" ("starting") material(s) are converted into "finished" ("product") material(s) in a macro context. In example, a team of operating technicians might be "starting up" "reactor" "Process Units" in a plant even as the team is also "doing maintenance" on a first "distillation tower" "Process Unit" and "running" a second "distillation tower" "Process Unit" disposed to operate in parallel with the first distillation tower. But it needs to also be appreciated that the "Process Units" do not stand free in a physically separated and defined manner in an apparatus such as a chemical manufacturing plant (the target use of the preferred embodiment) because the chemical manufacturing plant usually enables internal fluid movement by providing essentially one large apparatus built of conjoined vessels, pipes, pumps, valves, instruments, and wires. The "Process Unit" definitions are therefore, in verity, logical (in both cerebral and electrical-circuit-implemented contexts) and cultural rather than specifically and clearly physically defined. In example of this point, when a pipe with a valve connects a reactor to a surge tank, the reactor, pipe, valve, and surge tank are constructed as one unified and conjoined physical apparatus; one can conveniently consider the reactor as a first "Process Unit" and the surge tank as a second "Process Unit", but the issue of which Process

Unit includes the valve (and the pipe) for management and control purposes requires acceptance of the fact that a technologically artistic and cultural decision must be made since (a) there is no clear and specific physical separation between the two "Process Units" within the valve and (b) bifurcated control of the valve at a particular moment of real-time is definitely not desirable.

Hit List

Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs
Generate OACS				

Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 5774361 A

L30: Entry 1 of 2

File: USPT

Jun 30, 1998

US-PAT-NO: 5774361

DOCUMENT-IDENTIFIER: US 5774361 A

TITLE: Context sensitive vehicle alignment and inspection system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWIC	Draw
------	-------	----------	-------	--------	----------------	------	-----------	----------	--------	------	------

☐ 2. Document ID: US 5745727 A

L30: Entry 2 of 2

File: USPT

Apr 28, 1998

US-PAT-NO: 5745727

DOCUMENT-IDENTIFIER: US 5745727 A

TITLE: Linked caches memory for storing units of information

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KWIC	Draw
------	-------	----------	-------	--------	----------------	------	-----------	----------	--------	------	------

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
-------	---------------------	-------	----------	-----------	---------------

Terms	Documents
L29 and (link\$ with ind\$)	2

Display Format:

[Previous Page](#)

[Next Page](#)

[Go to Doc#](#)

Hit List

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs
Generate OACS				

Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 6650761 B1

L37: Entry 1 of 2

File: USPT

Nov 18, 2003

US-PAT-NO: 6650761

DOCUMENT-IDENTIFIER: US 6650761 B1

TITLE: Watermarked business cards and methods

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw. De
------	-------	----------	-------	--------	----------------	------	-----------	--------	------	----------

☐ 2. Document ID: US 6311214 B1

L37: Entry 2 of 2

File: USPT

Oct 30, 2001

US-PAT-NO: 6311214

DOCUMENT-IDENTIFIER: US 6311214 B1

TITLE: Linking of computers based on optical sensing of digital data

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw. De
------	-------	----------	-------	--------	----------------	------	-----------	--------	------	----------

Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
-------	---------------------	-------	----------	-----------	---------------

Terms	Documents
L36 and (search\$ with Internet)	2

Display Format:

[Previous Page](#)

[Next Page](#)

[Go to Doc#](#)